author	Krishna chaitanya chundru <quic_krichai@quicinc.com>	2023-02-28 17:19:12 +0530	
committer	Greg Kroah-Hartman <gregkh@linuxfoundation.org>	2023-03-30 12:51:41 +0200	
commit	e43bba938e2c9104bb4f8bc417ac4d7bb29755e1 (patch)		
tree	595664adbc62b07fcb9658239c0f9f384ac57640		
parent	2d77fbfe769c554d7802aa86a2f80402173964a2 (diff)		
download	linux-e43bba938e2c9104bb4f8bc417ac4d7bb29755e1.tar.gz		

arm64: dts: qcom: sc7280: Mark PCIe controller as cache coherent

```
commit 8a63441e83724fee1ef3fd37b237d40d90780766 upstream.

If the controller is not marked as cache coherent, then kernel will
try to ensure coherency during dma-ops and that may cause data corruption.
So, mark the PCIe node as dma-coherent as the devices on PCIe bus are
cache coherent.

Cc: stable@vger.kernel.org
Fixes: 92e0ee9f83b3 ("arm64: dts: qcom: sc7280: Add PCIe and PHY related node")
Signed-off-by: Krishna chaitanya chundru <quic_krichai@quicinc.com>
Signed-off-by: Bjorn Andersson <andersson@kernel.org>
Link: https://lore.kernel.org/r/1677584952-17496-1-git-send-email-quic_krichai@quicinc.com
Signed-off-by: Greg Kroah-Hartman <gregkh@linuxfoundation.org>
```

Diffstat

-rw-r--r-- arch/arm64/boot/dts/qcom/sc7280.dtsi 2

1 files changed, 2 insertions, 0 deletions

```
diff --git a/arch/arm64/boot/dts/qcom/sc7280.dtsi b/arch/arm64/boot/dts/qcom/sc7280.dtsi
index 3bedd45e14afdd..a407cd25797199 100644
--- a/arch/arm64/boot/dts/qcom/sc7280.dtsi
+++ b/arch/arm64/boot/dts/qcom/sc7280.dtsi
@@ -2122,6 +2122,8 @@
                         pinctrl-names = "default";
                         pinctrl-0 = <&pcie1_clkreq_n>;

+                        dma-coherent;
+
                         iommus = <&apps_smmu 0x1c80 0x1>;

                         iommu-map = <0x0 &apps_smmu 0x1c80 0x1>,
```